REMARKS

I. Introduction

Claims 1-23 are pending in this application, of which claims 1-4 are independent. Applicants acknowledge, with appreciation, the Examiner's indication that claims 5-14 and 21-23 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In this Amendment, claims 1-23 have been amended. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the present Amendment should be apparent throughout the written description of the specification.

II. Priority

The Examiner pointed out that Applicants have not filed a certified copy of Japanese patent application No. 2003-18428. The certified copy of the Japanese patent application was filed on August 11, 2004. Applicants respectfully request that the Examiner clarify the record by acknowledging receipt of the certified copies of the priority documents.

III. The Objection to the Claims

The Examiner asserted that claims 17-20 are in improper dependent form, and request to rewrite these claims. The Examiner asserted that the claims fail to further limit the subject matter of a previous claim. This objection is respectfully traversed.

Applicants invite the Examiner's attention to MPEP 608.01(n), III. INFRINGEMENT TEST, part of which is reproduced below:

> The test as to whether a claim is a proper dependent claim is that it shall include every limitation of the claim from which it depends (35 U.S.C. 112, forth

> paragraph) or in other words that it shall not conceivably be infringed by anything which would not also infringe the basic claim.
>
> The test for a proper dependent claim under the fourth paragraph of 35 U.S.C. 112 is whether the dependent claim includes every limitation of the claim from which it depends.
>
> The fact that a dependent claim which is otherwise proper might relate to a separate invention which would require a separate search or be separately classified from the claim on which it depends would not render it an improper dependent claim, although it might result in a requirement for restriction.

Applicants submit that claims 17-20 include every limitation of claims 1 and 3 from which they depend, respectively, and thus, claims 17-20 meet the requirement under 35 U.S.C. §112, forth paragraph. Withdrawal of the objection to claims 17-20 is, therefore, respectfully solicited.

In addition, claims 3 and 4 have been objected to because of informalities. Applicants have amended claims 3 and 4 to add the definition of the term "defined delay fault" which are delay faults assumed to exist in a semiconductor integrated circuit. The definition is well known among persons skilled in the art. For example, U.S. Patent No. 5,737,341, issued April 7, 1998, attached, describes that "13 designates a file of information on fault, in which faults are defined" and "[t]he fault to be subjected to a test here is a fault supposed and modeled based on the circuit under test and, more specifically, a stuck-at fault in which a signal line of the circuit is fixed to a logic value 0 or 1" (column 10, lines 29-33). U.S. Patent No. 5,084,876, issued January 28, 1992, attached, also describes that "it is necessary to define in advance the nature of the fault which is to be detected. For present purposes, it will be assumed that the fault to be detected is a stuck-at-1 fault on one of the bus lines" (column 8, lines 27-31). In addition, U.S. Patent Nos. 6,067,651, 6,308,293 and 6,865,706 describes the defined fault. Accordingly, withdrawal of the objection to claims 3 and 4 is respectfully solicited.

IV. The Rejection of the Claims

Claims 1-4 and 15-20 have been rejected under 35 U.S.C. §102(b) as being anticipated by Iyengar et al. The Examiner asserted that Iyengar et al. discloses delay test identically corresponding to what is claimed.

Claims 1, 2 and 15, 17 and 19

Applicants submit that Iyengar et al. does not disclose a method of evaluating the quality of test sequences for delay faults including all the limitations recited in independent claim 1. Specifically, Iyengar et al. does not disclose, among other things, that "of all defined delay faults which are delay faults assumed to exist in a semiconductor integrated circuit, a delay fault having a design delay value, which is a delay value of a signal path as designed at the time of designing a semiconductor integrated circuit, equal to or lower than a predetermined value are excluded from a test object," as recited in claim 1.

In the statement of the rejection, the Examiner asserted that Iyengar et al. teaches a method for detecting definite delay faults by computing a threshold (predetermined design delay value), and detecting the definite delay faults when delay faults exceed the threshold value (predetermined design delay value) (see paragraph 6 of the Office Action). However, Applicants emphasize that Iyengar's threshold is different from the "predetermined value," as recited in claim 1. The threshold in Iyengar et al. is a threshold with regard to delay time due to a fault, while the claimed predetermined value is a value with respect to a delay value derived from circuit design. Iyengar et al. intends to detect a fault with a size greater than threshold ε representing a fault size, whereas the claimed invention is configured for excluding a delay fault with a design delay value derived from circuit design equal to or lower than a predetermined

value. In short, Iyengar et al. addresses delay due to a fault, whereas the claimed invention addresses a delay due to circuit design, not a fault.

Applicants' position on Iyengar et al. is supported by, for example, the following sentences: "For each fault and test pattern, we compute a threshold ε such that this fault is detected if its size exceeds ε" and "The goal is to detect at each fault site a fault of any size greater than ε, for ε as small as possible" (see, Abstract, and the paragraph under the header "3. The Quantitative Model," respectively).

Accordingly, Iyengar et al. does not disclose a method of evaluating the quality of test sequences for delay faults including all the limitations recited in independent claim 1. The above discussion is applicable to independent claim 2. Dependent claims 15, 17 and 19 are also patentably distinguishable over Iyengar et al. at least because these claims include all the limitations recited in independent claim 1.

Claims 3, 4, 16, 18 and 20

It is submitted that Iyengar et al. does not disclose a method of evaluating the quality of test sequences for delay faults including all the limitations recited in independent claim 3. Specifically, Iyengar et al. does not disclose, among other things, that (1) each of defined delay faults which are delay faults assumed to exist in a semiconductor integrated circuit is weighted; and (2) a ratio of the total of the weights with respect to the "delay faults detected by the test sequences for delay faults" to the total of the weights with respect to the defined delay faults is set as a fault coverage, as recited in claim 3.

First, Iyengar et al. does not disclose limitation (1) because Iyengar et al. discloses that weight is defined only for detected faults, not defined delay faults. Second, Iyengar et al. does

not disclose limitation (2) because the reference discloses that the denominator of test quality is detected faults (see equation (18) at page 861 of Iyengar et al.).

Iyengar et al. provides a method to evaluate test quality for the detected faults according to used test pattern, where only detected faults are used as a denominator in calculating the test quality (see equation (18) at page 861 of Iyengar et al.). Accordingly, the undetected faults are not considered in calculating the test quality in Iyengar et al. It is, therefore, apparent that Iyengar et al. does not disclose setting "the total of the weights with respect to the defined delay faults [including detected faults and undetected faults]" to the denominator of equation (18).

In contrast, in the present invention, the fault coverage is considered on both the detected faults and undetected faults, which quantitatively shows an effective level of detected faults and undetected faults for all the faults. In claim 3, the denominator of fault coverage is "the total of the weights with respect to the defined delay faults" to consider detected faults and undetected faults for all the faults.

Accordingly, Iyengar et al. does not disclose a method of evaluating the quality of test sequences for delay faults including all the limitations recited in independent claim 3. The above discussion is applicable to independent claim 4. Dependent claims 16, 18 and 20 are also patentably distinguishable over Iyengar et al. at least because these claims include all the limitations recited in independent claim 3.

Applicants, therefore, respectfully solicit withdrawal of the rejection of claims 1-4 and 15-20 under 35 U.S.C. §102(b) as evidenced by Iyengar et al., and favorable consideration thereof.

V. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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